Amendment to the Claims:

1 (currently amended): A method of cell placement and clock tree synthesis comprising steps of:

(a) identifying critical paths in an integrated circuit design;

(b) partitioning the integrated circuit design into a timing group for each of the critical paths wherein each timing group includes only critical paths;

(c) assigning each flip-flop in a critical path to a timing group corresponding to the critical path;

(d) performing a cell placement to minimize a function of propagation delay and maximum distance between flip-flops within each timing group; and

(e) constructing a clock sub-net for each timing group.

2 (original): The method of Claim 1 wherein each timing group contains only flip-flops that are included in a critical path.

3 (original): The method of Claim 1 further comprising a step of replacing a flip-flop in a critical path with a flip-flop in a non-critical path connected to the critical path.

4 (original): The method of Claim 3 further comprising a step of inserting a clock skew between the critical path and the non-critical path.

5 (original): The method of Claim 1 wherein flip-flops in connected critical paths are assigned to the same

timing group.

6 (original): The method of Claim 1 wherein every flip-flop that is included in a critical path is assigned to a timing group.

7 (original): The method of Claim 1 further comprising a step of coupling a clock buffer to the clock sub-net so that the clock buffer is equidistant from each flip-flop in the timing group.

8 (original): The method of Claim 7 further comprising a step of coupling a clock signal to the clock buffer from a clock tree.

9 (original): The method of Claim 7 wherein the clock tree is a balanced clock tree.

10 (currently amended): A computer program product for cell placement and clock tree synthesis comprising:

a medium for embodying a computer program for input to a computer; and

a computer program embodied in the medium for causing the computer to perform steps of:

(a) identifying critical paths in an integrated circuit design;

(b) partitioning the integrated circuit design into a timing group for each of the critical paths;

(c) assigning each flip-flop in a critical path to a timing group corresponding to the critical path wherein each timing group includes only critical paths;

(d) performing a cell placement to minimize a function of

propagation delay and maximum distance between flip-flops within each timing group; and

(e) constructing a clock sub-net for each timing group.

11 (original): The computer program product of Claim 10 wherein each timing group contains only flip-flops that are included in a critical path.

12 (original): The computer program product of Claim 10 further comprising a step of replacing a flip-flop in a critical path with a flip-flop in a non-critical path connected to the critical path.

13 (original): The computer program product of Claim 12 further comprising a step of inserting a clock skew between the critical path and the non-critical path.

14 (original): The computer program product of Claim 10 wherein flip-flops in connected critical paths are assigned to the same timing group.

15 (original): The computer program product of Claim 10 wherein every flip-flop that is included in a critical path is assigned to a timing group.

16 (original): The computer program product of Claim 10 further comprising a step of coupling a clock buffer to the clock sub-net so that the clock buffer is equidistant from each flip-flop in the timing group.

17 (original): The computer program product of Claim 16 further comprising a step of coupling a clock signal

to the clock buffer from a clock tree.

18 (original): The computer program product of Claim 17 wherein the clock tree is a balanced clock tree.